

Appl. No. 10/709,569
Amdt. dated May 10, 2005
Reply to Office action of March 11, 2005

Listing of Claims:

Claim 1 (previously presented): A bipolar junction transistor, comprising:

- a substrate;
- a dielectric layer formed on the substrate;
- 5 an opening formed in the dielectric layer to expose a portion of the substrate;
- a selective implant collector region formed in the substrate and beneath the opening;
- a heavily doped polysilicon layer formed on a sidewall of the opening to define a self-aligned base region in the opening;
- an intrinsic base doped region positioned in a bottom of the opening and within the
- 10 self-aligned base region defined by the heavily doped polysilicon layer;
- a spacer formed on the heavily doped polysilicon layer to define a self-aligned emitter region in the opening; and
- an emitter conductivity layer being filled within the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer and the intrinsic base
- 15 doped region.

Claim 2 (original): The bipolar junction transistor of claim 1, wherein the heavily doped polysilicon layer comprises a boron dopant with a dosage ranging from $1\text{E}19$ to $1\text{E}21$ atoms/cm².

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Claim 3 (original): The bipolar junction transistor of claim 1, wherein the substrate is a silicon substrate.

Claim 4 (original): The bipolar junction transistor of claim 1, wherein the substrate is a non-selective epitaxial silicon substrate.

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Claim 5 (original): The bipolar junction transistor of claim 1, further comprising a salicide layer formed on the emitter conductivity layer.

Appl. No. 10/709,569
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Claim 6 (canceled)

5 Claim 7 (original): The bipolar junction transistor of claim 1, further comprising an extended conductivity layer formed on the dielectric layer to connect to the heavily doped polysilicon layer.

10 Claim 8 (original): The bipolar junction transistor of claim 7, further comprising an oxide layer and a silicon nitride layer formed between the extended conductivity layer and the dielectric layer.

Claim 9 (original): The bipolar junction transistor of claim 7, wherein the extended conductivity layer is composed of in-situ doped polysilicon.

15 Claim 10 (original): The bipolar junction transistor of claim 7, further comprising a salicide layer formed on the extended conductivity layer.

20 Claim 11 (original): The bipolar junction transistor of claim 1, wherein the substrate further comprises at least a deep isolation trench.

Claim 12 (original): The bipolar junction transistor of claim 11, wherein the substrate further comprises at least a channel stop region formed in the bottom of the deep isolation trench.

25 Claim 13 (original): The bipolar junction transistor of claim 1, wherein the intrinsic base doped region comprises a boron dopant.

Claim 14 (previously presented): A bipolar junction transistor, comprising:

Appl. No. 10/709,569
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- a substrate;
- at least a deep isolation trench formed in the substrate and at least a channel stop region formed in the bottom of the deep isolation trench;
- a dielectric layer formed on the substrate;
- 5 an opening formed in the dielectric layer to expose a portion of the substrate;
- a doped polysilicon layer formed on a sidewall of the opening and on the dielectric layer outside of the opening, the doped polysilicon layer defining a self-aligned base region in the opening;
- an intrinsic base doped region positioned in a bottom of the opening and within the
- 10 self-aligned base region defined by the doped polysilicon layer;
- a spacer formed on the doped polysilicon layer to define a self-aligned emitter region in the opening; and
- an emitter conductivity layer being filled within the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer and the intrinsic base
- 15 doped region.

Claim 15 (original): The bipolar junction transistor of claim 14, wherein the doped polysilicon layer comprises a boron dopant.

- 20 Claim 16 (original): The bipolar junction transistor of claim 14, further comprising a salicide layer formed on the emitter conductivity layer and on the portion of the doped polysilicon layer outside of the opening.

- Claim 17 (original): The bipolar junction transistor of claim 14, further comprising a
- 25 selective implant collector (SIC) region formed in the substrate beneath the intrinsic base doped region.

Claim 18 (canceled)

Appl. No. 10/709,569
Amdt. dated May 10, 2005
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Claim 19 (canceled)

Claim 20 (original): The bipolar junction transistor of claim 14, wherein the intrinsic base
5 doped region comprises a boron dopant.

Claim 21 (previously presented): A bipolar junction transistor, comprising:

- a substrate;
- at least a deep isolation trench formed in the substrate and at least a channel stop
10 region formed in the bottom of the deep isolation trench;
- a dielectric layer formed on the substrate;
- an opening formed in the dielectric layer to expose a portion of the substrate;
- a heavily doped polysilicon layer formed on a sidewall of the opening to define a
self-aligned base region in the opening;
- 15 an intrinsic base doped region positioned in a bottom of the opening and within the
self-aligned base region defined by the heavily doped polysilicon layer;
- a spacer formed on the heavily doped polysilicon layer to define a self-aligned
emitter region in the opening; and
- an emitter conductivity layer being filled within the self-aligned emitter region, and
20 a PN junction being formed between the emitter conductivity layer and the intrinsic base
doped region.